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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,904	01/24/2001	Lap-Wai Chow	B-3964 618029-8	4228

36716 7590 03/18/2005

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EXAMINER

NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

In view of the Appeal Brief filed on 02/27/2005, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-16 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al..

Regarding claim 9, Liu et al. discloses on figure 7 a semiconductor device adapted to prevent and/or thwart reverse engineering comprising field oxide layer 12 disposed on a semiconductor substrate 10; a metal plug contact 24 disposed outside a contact region 19 and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and a metal 26 connected to said metal plug contact 24.

Regarding claim 10, Liu et al. discloses on figure 7 said semi-conducting device comprises integrated circuit (col. 1, lines 19-25).

Regarding claim 11, Liu et al. discloses on figure 7 said filed oxide layer 12 further comprises silicon oxide (col. 4, lines 48-50).

Regarding claim 12, Liu et al. discloses on figure 7 said integrated circuits further comprise complementary metal oxide semiconductor integrated circuits and bipolar silicon based integrated circuits (col. 1, lines 19-25).

Regarding claim 13, Liu et al. discloses on figure 7 a method for preventing and/or thwarting reverse engineering comprising steps of providing a field oxide layer 12 disposed on a semiconductor substrate 10; providing a metal plug contact 24 disposed outside a contact region 19 and above said field oxide layer 12, wherein said metal plug metal is electrically isolated from said contact region; and connecting a metal 26 to said metal plug contact 24.

Regarding claim 14, Liu et al. discloses on figure 7 said semi-conducting device comprises integrated circuit (col. 1, lines 19-25).

Regarding claim 15, Liu et al. discloses on figure 7 said filed oxide layer 12 further comprises silicon oxide (col. 4, lines 48-50).

Regarding claim 16, Liu et al. discloses on figure 7 said integrated circuits further comprise complementary metal oxide semiconductor integrated circuits (col. 1, lines 19-25).

Regarding claim 19, Liu et al. discloses on figure 7 said filed oxide layer 12 has an uppermost side, said metal plug contact 24 being deposited on said uppermost side of said field oxide layer.

Regarding claim 20, Liu et al. discloses on figure 7 said filed oxide layer 12 has an uppermost side, said metal plug contact 24 being deposited on said uppermost side of said field oxide layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
March 15, 2005



ALLAN R. WILSON
PRIMARY EXAMINER